REMARKS/ARGUMENT

Claims 1-19 were examined in the most recent Office Action. Claims 1-19 stand rejected. Claims 1-2, 4, 7 and 16-18 are amended. Accordingly, claims 1-19 are pending in the present application. No new matter is added.

Applicants acknowledge with thanks the thorough search and examination conducted by the Examiner. A response to the Examiner's observation follows.

Claim Rejections - 35 U.S.C. §102

Claim 16 is rejected under 35 U.S.C. §102(e) as being anticipated by Miyasaka (U.S. Patent No. 6,124,154). In particular, the Office Action states that Miyasaka shows all the elements of the present invention recited in claim 16. Applicants respectfully traverse the rejection.

Claim 16 is amended to recite that the thermally deposited silicon oxide gate dielectric layer has a thickness of from about 500 to 700Å. The disclosure by Miyasaka discusses only formation of a gate insulator layer, and contains no disclosure regarding the critical thickness of the gate insulator layer. Accordingly, Applicants respectfully submit that claim 16 contains elements not shown in the cited prior art reference. Accordingly, Applicants believe that the rejection of claim 16 under 35 U.S.C. §102(e) is overcome, and requests that it be reconsidered and withdrawn.

Claim Rejections - 35 U.S.C. §103

Claims 1-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Huang et al. (U.S. Patent No. 6,037,199) in view of Doklan et al. (U.S. Patent No. 4,851,370). In particular, the Office Action states that the teachings in Huang et al. and Doklan et al. would make the present invention obvious to one of ordinary skill in the art. The rejection is respectfully traversed.

First, Applicants note that independent claims 1, 7 and 16 are amended to recite that the thin film transistor (TFT) according to the present invention is formed with a polysilicon layer on an insulating substrate, and with either a single or composite gate dielectric layer atop the

polysilicon layer. In addition, the single or composite gate dielectric layer is formed to have a thickness of from about 550 to 850Å.

Second, the disclosure by Huang et al. specifically calls for a semiconductor layer that is a single crystalline silicon that is overlaid with a gate dielectric layer. Huang et al. failed to disclose a polysilicon layer that is overlaid by a gate dielectric layer (col. 3, lines 6-53).

Third, Huang et al. disclose that the gate dielectric layer overlaid on the single crystalline silicon layer has a thickness of about 30 to 100Å (col. 3, line 67-col. 4, line 5).

Fourth, the disclosure by Doklan et al. contains no apparent disclosure of the state of the silicon substrate, i.e., whether the silicon is single crystalline or polycrystalline. Doklan et al. discuss the substrate only as a platform for forming a gate dielectric layer.

Fifth, the disclosure by Doklan et al. fails to show or discuss the thickness of the gate dielectric layer, noting only that a first thermal oxide layer is approximately 5nm thick. The disclosure by Doklan et al. is silent with regard to the thickness of the overall gate dielectric layer.

Applicants note that claims 1, 7 and 16 all recite that the TFT of the present invention is constructed using a polysilicon, or polycrystalline silicon, layer rather than a single crystalline silicon layer. In addition, each of these claims recite that the gate dielectric layer has a thickness of from about 550 to 850Å. None of the cited prior art references, either alone or in combination appear to disclose the use of a polysilicon layer on an insulating substrate, and further appear to lack any disclosure regarding the increased thickness of the gate dielectric layer. Instead, each of the above references call for a single crystalline silicon structure underlying the gate dielectric layer. It should be noted that single crystalline silicon is much smother than polysilicon, and does not provoke the same problems and issues as are addressed by the invention in claims 1, 7 and 16 of the present application.

Applicants note that the thickness of the gate dielectric layer is critical to the present invention and in particular with the annealing steps in which the polysilicon crystals will typically increase in size. Indeed, the disclosure by Doklan et al. appears to focus on reducing the thickness of the gate dielectric layer, and thus teaches away from the critical features of the present invention.

In adddition, it appears that none of the cited prior art references identifies the problems encountered in a TFT where a rough polysilicon surface is overlaid by a gate dielectric layer. Applicants therefore respectfully submit that claims 1, 7 and 16 contain elements that are neither disclosed nor suggested by the cited prior art references, either alone or in combination. Accordingly, Applicants respectfully request that the rejection of claims 1, 7 and 16 under 35 U.S.C. §103(a) over the combination of Huang et al. and Doklan et al. be reconsidered and withdrawn.

Claims 2-6, 8-15 and 17-19 depend upon and further limit the above independent claims, and should be allowable for that reason and because they contain further limitations in each claim. Reconsideration of the rejection of these claims under 35 U.S.C. §103(a) and withdrawal of the rejection is respectfully requested.

Claims 17-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Miyasaka. In particular, the Office Action states that the Examiner takes official notice that the specific processing conditions with respect to the polysilicon layer and the thermal oxidation and densification are typical well known processing conditions. The rejection is respectfully traversed.

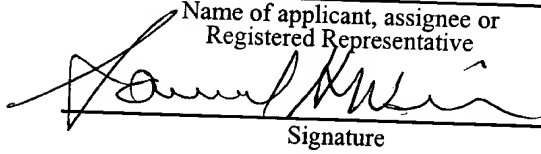
As discussed above, with regard to the disclosures by Huang et al. and Doklan et al., and in the anticipation rejection of claim 16, a rough polysilicon layer overlaid by a gate dielectric layer having a thickness of from about 550 to 850Å is not shown or suggested in the disclosure by Miyasaka. Although the Examiner takes official notice that these parameters are well known processing conditions, the cited prior art references have failed to disclose any teaching or suggestion with regard to formation of the thick gate dielectric layer. In other words, Applicants respectfully submit that the present invention recited in claims 17-19 can only be arrived at through efforts that extend far beyond routine experimentation. That is, none of the prior art recognizes the use of a rough polysilicon layer overlaid with a thick gate dielectric layer as a result effective variable for the problems presented in the present invention. MPEP §214404IIB. Accordingly, Applicants respectfully request that the rejection of claims 17-19 under 35 U.S.C. §103(a) based on the disclosure by Miyasaka be reconsidered and withdrawn.

Conclusion

Applicants respectfully submit that the foregoing response addresses all issues raised in the most recent Office Action. In addition, in view of the above discussion and amendments, Applicants respectfully believe that the application is now in condition for allowance, and earnestly solicits notice to that effect. If it is believed that progress on the prosecution of the application can be made with a telephonic interview, the Examiner is requested to contact the undersigned counsel at the number provided below.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on October 28, 2002:

Samuel H. Weiner
Name of applicant, assignee or Registered Representative



Signature

October 28, 2002
Date of Signature

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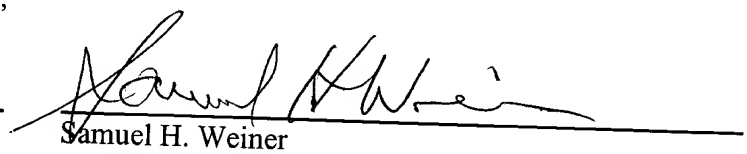
Respectfully submitted,



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APPENDIX A

"CLEAN" VERSION OF EACH PARAGRAPH/SECTION/CLAIM

37 C.F.R. § 1.121(b)(ii) AND (c)(i)

CLAIMS (with indication of amended or new):

1. (Amended) A method of forming a composite gate dielectric layer for a thin film transistor (TFT), device, comprising the steps of:

providing an insulating substrate;

providing a polysilicon layer on said insulating substrate;

thermally growing a first gate dielectric layer, in a furnace, on said polysilicon layer;

B1

performing a first anneal procedure to change said polysilicon layer;

thermally depositing a second gate dielectric layer on said first gate dielectric layer; and

performing a second anneal procedure to create a densified second gate dielectric layer, resulting in said composite gate dielectric layer comprised of said densified second gate dielectric on said first gate dielectric layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms.

2. (Amended) The method of claim 1, wherein said polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD) procedures to a thickness of from about 500 to 1000 Angstroms.

B2

4. (Amended) The method of claim 1, wherein said first anneal procedure, used to change said polysilicon layer, is performed at a temperature between about 900 to 1200°C, in a nitrogen or argon ambient, for a time between about 3 to 5 hrs.

7. (Amended) A method forming a thin film transistor, featuring a composite gate dielectric layer, on an insulating substrate, comprising the steps of:

B3

providing said insulating substrate;

forming a first polysilicon layer on said insulating substrate;

thermally growing a first silicon oxide layer, in a furnace, on said polysilicon layer;

performing a first anneal procedure, in situ in said furnace, to improve TFT parametric performance;

thermally depositing a second silicon oxide gate dielectric layer, on underlying, said first silicon oxide dielectric layer, via thermal decomposition of tetraethylorthosilicate (TEOS),

performing a second anneal procedure to densify said second silicon oxide gate dielectric layer, resulting in said composite gate dielectric layer, comprised of densified, said second silicon oxide gate dielectric layer on said first silicon oxide gate insulator layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms;

depositing a second polysilicon layer;

patterning of said second polysilicon layer, and of said composite gate dielectric layer to create a polysilicon gate structure on said composite gate dielectric layer; and

forming a source/drain region in a portion of said first polysilicon layer, not covered by said polysilicon gate structure.

16. (Amended) A method of forming a thermally deposited, gate dielectric layer, for a thin film transistor device, comprising the steps of:

providing said insulating substrate;

forming a polysilicon layer on said insulating substrate;

thermally depositing a silicon oxide gate dielectric layer on said polysilicon layer, using tetraethylorthosilicate as a source to a thickness of from about 500 to 700 Angstroms; and

performing an anneal procedure to densify said silicon oxide gate dielectric layer.

17. (Amended) The method of claim 16, wherein said polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD) procedures to a thickness of from about 500 to 1500 Angstroms.

18. (Amended) The method of claim 16, wherein said silicon oxide gate dielectric layer is deposited at a temperature between about 600 to 700°C.

APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

CLAIMS:

1. (Amended) A method of forming a composite gate dielectric layer for a thin film transistor (TFT), device, comprising the steps of:

providing an insulating substrate;

providing [an active semiconductor] a polysilicon layer on said insulating substrate;

thermally growing a first gate dielectric layer, in a furnace, on said [active semiconductor layer] polysilicon layer;

performing a first anneal procedure to change said [active semiconductor layer] polysilicon layer;

thermally depositing a second gate dielectric layer on said first gate dielectric layer; and

performing a second anneal procedure to create a densified second gate dielectric layer, resulting in said composite gate dielectric layer comprised of said densified second gate dielectric on said first gate dielectric layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms.

2. (Amended) The method of claim 1, wherein said [active semiconductor layer is a] polysilicon layer[,] is obtained via low pressure chemical vapor deposition (LPCVD)[,] procedures[,] to a thickness [between] of from about 500 to 1000 Angstroms.

4. (Amended) The method of claim 1, wherein said first anneal procedure, used to change said [active semiconductor] polysilicon layer, is performed at a temperature between about 900 to 1200°C, in a nitrogen or argon ambient, for a time between about 3 to 5 hrs.

7. (Amended) A method forming a thin film transistor, featuring a composite gate dielectric layer, on an insulating substrate, comprising the steps of:

providing said insulating substrate;

forming a first polysilicon layer on said insulating substrate;

thermally growing a first silicon oxide layer, in a furnace, on said polysilicon layer;

performing a first anneal procedure, in situ in said furnace, to improve TFT parametric performance;

thermally depositing a second silicon oxide gate dielectric layer, on underlying, said first silicon oxide dielectric layer, via thermal decomposition of tetraethylorthosilicate (TEOS),

performing a second anneal procedure to densify said second silicon oxide gate dielectric layer, resulting in said composite gate dielectric layer, comprised of densified, said second silicon oxide gate dielectric layer on said first silicon oxide gate insulator layer, said composite gate dielectric layer having a thickness of from about 550 to 850 Angstroms;

depositing a second polysilicon layer;

patterning of said second polysilicon layer, and of said composite gate dielectric layer to create a polysilicon gate structure on said composite gate dielectric layer; and

forming a source/drain region in a portion of said [large grain size] first polysilicon layer, not covered by said polysilicon gate structure.

16. (Amended) A method of forming a thermally deposited, gate dielectric layer, for a thin film transistor device, comprising the steps of:

providing said insulating substrate;

forming [an active semiconductor] a polysilicon layer on said insulating substrate;

thermally depositing a silicon oxide gate dielectric layer on said [active semiconductor] polysilicon layer, using tetraethylorthosilicate as a source to a thickness of from about 500 to 700 Angstroms; and

performing an anneal procedure to densify said silicon oxide gate dielectric layer.

17. (Amended) The method of claim 16, wherein said [active semiconductor layer is a] polysilicon layer[,] is obtained via low pressure chemical vapor deposition (LPCVD)[,] procedures[,] to a thickness of from [between] about 500 to 1500 Angstroms.

18. (Amended) The method of claim 16, wherein said silicon oxide gate dielectric layer [is a thermally deposited silicon oxide layer, obtained at a thickness between about 500 to 700 Angstroms,] is deposited at a temperature between about 600 to 700°C[, using tetraethylorthosilicate as a source].